Q.P. Code: 16EC402 **R16**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech III Year I Semester Supplementary Examinations August-2022

SWITCHING THEORY AND LOGIC DESIGN

(Electrical and Electronics Engineering)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	**a**	Simplify the following Boolean expression: (a) F = (A+B) (A'+C) (B+C).	**L4**	**6M**
	b	(b) F = A+B+C'+D (E+F).	**L4**	**6M**
		OR		
2	**a**	Convert the following to binary and then to gray code. (i) (1111)16 (ii) (BC54)16 (iii) (237)8 (iv) (164)10 (v) (323)8	**L2**	**6M**
	b	Perform the following using BCD arithmetic (i) (79)10 + (177)10 (ii) (481)10 + (178)10	**L2**	**6M**

UNIT-II

3	**a**	Minimize the following Boolean function using K-Map F(A, B, C, D)= Σm(0, 2, 4, 6, 8, 10, 12, 14).	**L4**	**6M**
	b	Realize it using NAND Gates.	**L4**	**6M**
		OR		
4		Simplify the following Boolean function using Tabulation method Y(A,B,C,D) = Σ(1,3,5,8,9,11,15)	**L4**	**12M**

UNIT-III

5	**a**	Design & implement Full Adder with truth table.	**L6**	**6M**
	b	Design & implement Full Subtractor with truth table.	**L6**	**6M**
		OR		
6		Implement 4-bit Magnitude Comparator and write down its design procedure.	**L6**	**12M**

UNIT-IV

7	**a**	Draw the logic symbol, characteristics table and derive characteristics equation of JK flip flop.	**L4**	**6M**
	b	Design T Flip Flop by using JK Flip Flop and draw the timing diagram.	**L6**	**6M**
		OR		
8		Implement 6-bit ring counter using suitable shift register. Briefly describe its operation.	**L6**	**12M**

UNIT-V

9		Implement the following Boolean function using PLA (i)F(w,x,y,z) = Σm(0,1,3,5,9,13) (ii)F(w,x,y,z)) = Σm(0,2,4,5,7,9,11,15)	**L6**	**12M**
		OR		
10		Discuss Mealy & Moore Machine models of sequential machines.	**L3**	**12M**

*** END ***